



8085 INVERSE ASSEMBLER

OPERATING NOTE/APRIL 1986

Introduction

This Operating Note includes information for using the 8085 Inverse Assembler with the Model 10269B and Model 64655A Processor Interface Module or using the "8085 Inverse Assembler for Probes" without the 10269B or preprocessor module.

Using the 10269B General Purpose Probe Interface.

The Model 64655A Processor Interface Module, when installed in the Model 10269B General Purpose Probe Interface, provides a complete interface between any 8085 target system and the Model 1630A/D/G or 1631A/D Logic Analyzer. The interface module connects signals from the 8085 target microprocessor to the logic analyzer inputs, along with all of the status and clock signals required for inverse assembly of the 8085 instruction set.

The 8085 configuration software on the flexible disc sets up the logic analyzer format specification for compatibility with the 8085 microprocessor, and assigns names to values found on the 8085 status bus. It also contains the inverse assembler routine required to obtain displays of 8085 data in assembly language mnemonics. The interface module specifications are given in table 1.

Table 1. Interface Module Specifications

Processor Compatibility:	Intel 8085 and all microprocessors made by other manufacturers which comply with Intel 8085 specifications.
Maximum Clock Speed:	6 MHz clock output from microprocessor.
Signal Line Loading:	One LS TTL load for all monitored signal lines plus approx 35 pF capacitance.
Power Consumption:	0.30 A at +5Vdc max, supplied by Model 1630A/D/G or 1631A/D Logic Analyzer.
Environmental	
Temperature:	Operating, 0 to +55 degrees C (+32 to +131 degrees F); Nonoperating, -40 to +75 degrees C (-40 to +167 degrees F).
Altitude:	Operating, 4600 m (15 000 ft); Nonoperating, 15 300m (50 000 ft).
Humidity:	To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

Operating Note Part No. 10304-90904
Microfiche Part No. 10304-90804



System Configuration

The minimum hardware required for state analysis of an 8085 target system consists of the following:

- a. Model 1630A/D/G or 1631A/D Logic Analyzer with HP 9121D/S or HP 9122D/S 3 1/2" Flexible Disc Drive.
- b. 10269B General Purpose Probe Interface with Model 10304B 8085 Preprocessor which includes:
 1. 64655A Interface Module for 8085 microprocessors, including an 8085 interface circuit card and cable assembly.
 2. 8085 Inverse Assembler and format specification setups on Flexible Disc HP Part No. 10304-13012.
- c. BNC cable assembly to connect +5V accessory power from logic analyzer to general purpose probe interface.

Hardware Installation

Install the interface module on the underside of the general purpose probe interface pod. Insert the free end of the interface card into the slots of the pod, then connect the pod internal cables to the interface circuit card, and fasten the cable end of the interface module to the pod using two screws.

Connect a BNC cable from the ACCESSORY POWER output on the rear panel of the logic analyzer to the ACCESSORY POWER input on the general purpose probe interface.

Note

Some interface modules can draw up to 1 ampere from the 5-volt supply. If using coaxial cable, HP recommends that you use RG-58, 4-foot or less to minimize voltage drop.

Connect the interface cable to the target system by lifting the 8085 CPU from its socket, plug the interface cable into the CPU socket, and plug the CPU into the interface cable.

CAUTION

Care must be taken to align pin 1 of the cable assembly with pin 1 of the processor socket on the target system board.

Pin 1 of the cable socket is identified on the CPU socket board and shown in figure 1.

The CPU socket on the interface cable is a Zero Insertion Force (ZIF) socket. Before installing the CPU, open the socket by rotating the small screw located at the pin 1 end of the socket. To secure the CPU in the socket, rotate the screw in the opposite direction.

To obtain a lower profile assembly, the probe cable can be used without the ZIF socket. Figure 1 is an exploded view of the socket assembly. Separate the ZIF socket assembly by inserting a flat blade screw driver under the pc board located directly below the ZIF socket and carefully prying up. Avoid bending the pins of the ZIF socket or probe cable assembly. Plug the probe assembly into the target system, and install the CPU in the cable socket. The plastic pin guard can be removed if it interferes with components of the target system, or if an even lower profile is required. Removal of the pin guard is not recommended, however, because this increases the danger of damage to the probe pins.

Interface Requirements

The 8085 Interface Module will operate with an 8085 microprocessor clocked at rates up to 6 MHz. The Interface Module adds one LS TTL load to all monitored lines (excludes 8085 clock pins 1 and 2) an interface capacitance of approximately 35 pF.

Performance Verification and Adjustment Procedures.

There are no automatic performance tests and no adjustments for the Model 64655A Preprocessor Module.

Troubleshooting

If a failure is suspected in the HP 64655A Preprocessor Interface Module consult your nearest Hewlett-Packard Sales/Service office for information concerning repair of the board.

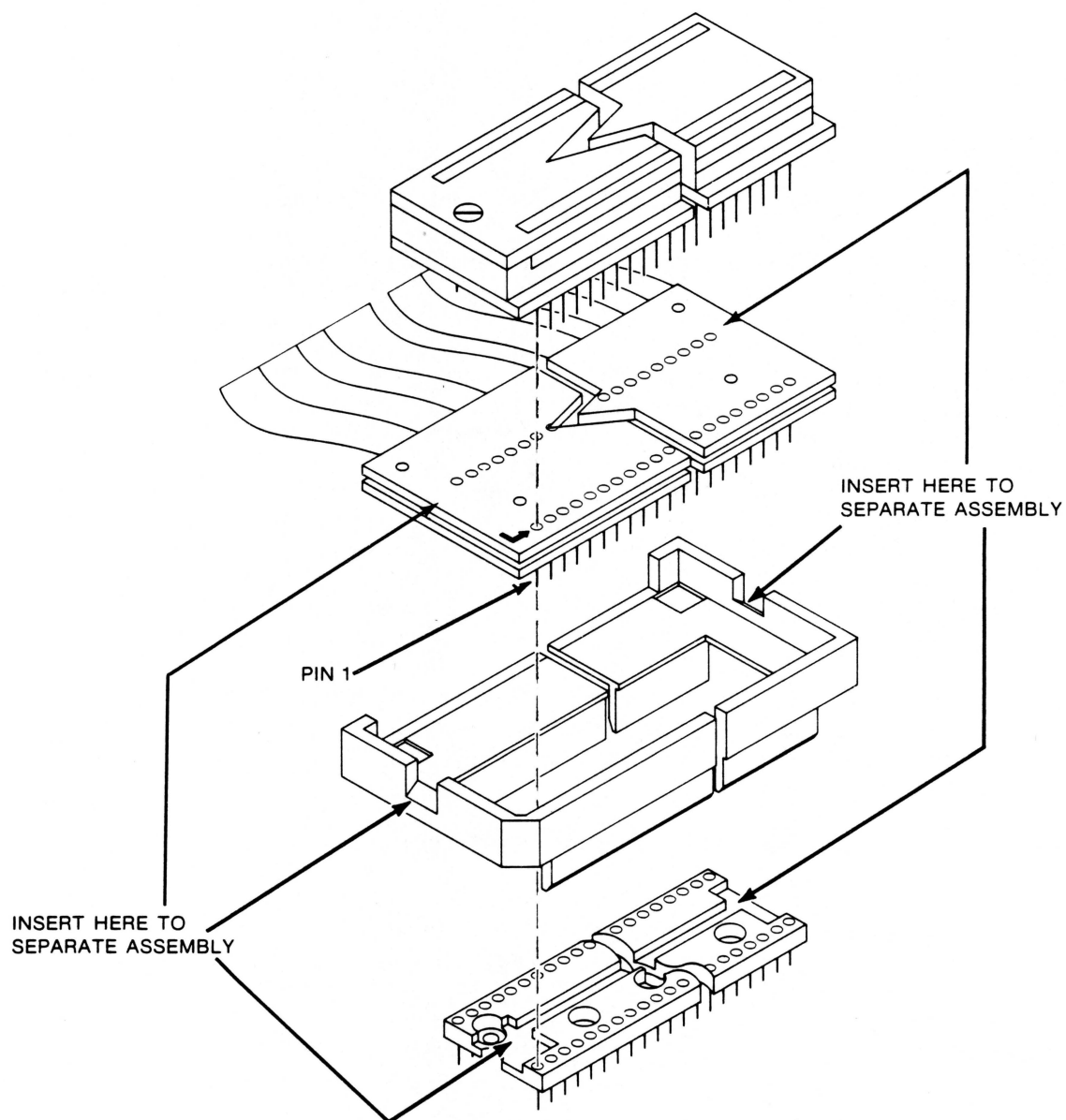


Figure 1. ZIF Socket Assembly, Exploded View

Connect the 1630A/D/G or 1631A/D Logic Analyzer pods to the general purpose probe interface (Model 10269B) as follows:

Model 10269B Connector	1630A/D & 1631A/D Pod	Model 1630G Pod
A	1	5
B	4	4
C	2	2
D	3	3
E	n/c	n/c
F	n/c	n/c
G	n/c	n/c
H	n/c	n/c

Interface Description

The 8085 interface circuit is comprised of buffers and NAND gates. Generation and gating of some status signals to the general purpose probe interface is performed by the NAND gates. Figure 2 shows the 8085 interface block diagram.

Table 2 lists the CPU signals and cable lines on which those signals are carried to the logic analyzer.

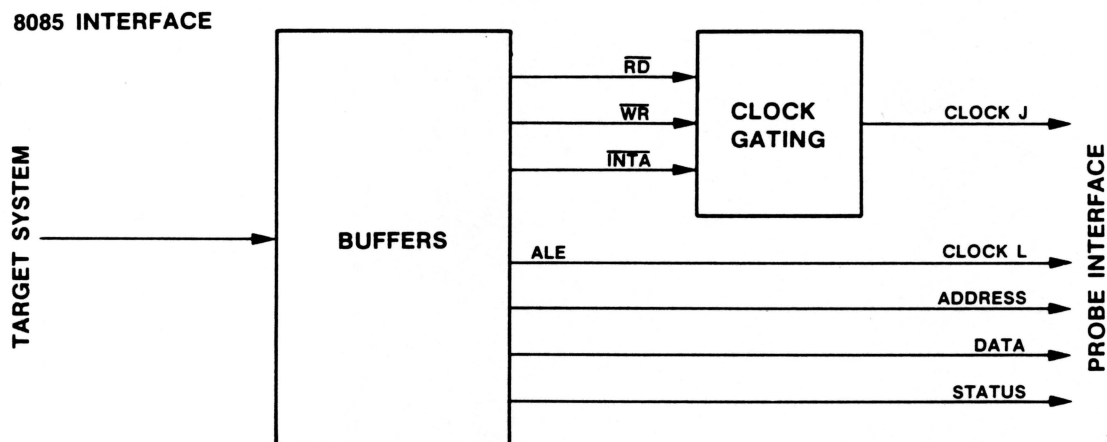


Figure 2. 8085 Interface Block Diagram

Table 2. 8085 Signal List

CPU SIGNAL	CPU PIN	LABEL	1630A/D & 1631A/D		1630G	
			POD	BIT	POD	BIT
AD0	12	ADDRESS	2	0	2	0
AD1	13	ADDRESS	2	1	2	1
AD2	14	ADDRESS	2	2	2	2
AD3	15	ADDRESS	2	3	2	3
AD4	16	ADDRESS	2	4	2	4
AD5	17	ADDRESS	2	5	2	5
AD6	18	ADDRESS	2	6	2	6
AD7	19	ADDRESS	2	7	2	7
A8	21	ADDRESS	2	8	2	8
A9	22	ADDRESS	3	0	3	0
A10	23	ADDRESS	3	1	3	1
A11	24	ADDRESS	3	2	3	2
A12	25	ADDRESS	3	3	3	3
A13	26	ADDRESS	3	4	3	4
A14	27	ADDRESS	3	5	3	5
A15	28	ADDRESS	3	6	3	6
AD0	12	DATA	1	0	5	0
AD1	13	DATA	1	1	5	1
AD2	14	DATA	1	2	5	2
AD3	15	DATA	1	3	5	3
AD4	16	DATA	1	4	5	4
AD5	17	DATA	1	5	5	5
AD6	18	DATA	1	6	5	6
AD7	19	DATA	1	7	5	7
S0	29	STATUS	4	0	4	0
S1	33	STATUS	4	1	4	1
HLDA	38	STATUS	4	2	4	2
IO/LM	34	STATUS	4	3	4	3
ALE	30		2	L clk	2	L clk
NAND OF:			4	J clk	4	J clk
INTA	11					
WR	31					
RD	32					

Operation

The logic analyzer will be configured for state analysis when you load the inverse assembler from the flexible disc.

To load the inverse assembler from the flexible disc select the system menus and press NEXT[], PREV[] keys until the [Storage Operations] menu is displayed. Press the ROLL keys until the cursor (>) is next to the file name "I8085IP". Once the file has been found, the NEXT[], PREV[] keys must be pressed until the [Load] function is selected, then press insert to actually load the file into the 1630.

FORMAT SPECIFICATION

When using the 8085 interface module, the format specification will be set up by the flexible disc software as shown in figures 3 and 4.

State Format Specification _____										
[Assignment]		Slave Clock			Master Clock					
		JKL			JKL					
		[.]↓.....			[.]↓.....					
Multiplexing	Pod4	Pod3	Pod2	Pod1	Pod0					
[27/8]	[TTL]	[TTL]	[TTL]	[TTL]	[TTL]					
	8.....0	8.....0	8.....0	7.....0	7.....0					
Activity>										
Label	Pol									
ADDR	[+]	[.....]	..*****	*****						
DATA	[+]	[.....]			*****					
STAT	[+]	[.....]	*****							

Figure 3. 8085 Format Specification for 1630A/D and 1631A/D

State Format Specification _____										
[Assignment]		Slave Clock JKL [...↓]			Master Clock JKL [↓...]					
		Master	Slave	Slave	Slave	Master				
Multiplexing		Pod5	Pod4	Pod3	Pod2	Pod1				
[27/38]		[TTL]	[TTL]	[TTL]	[TTL]	[TTL]				
		9.....0	8.....0	8.....0	8.....0	7.....0				
Activity>										
Label		Pol								
ADDR	[+]	[..... ***** ..]								
DATA	[+]	[.. ***** ..]								
STAT	[+]	[..... **** ..]								

Figure 4. 8085 Format Specification for 1630G

Inputs to the logic analyzer are grouped under functional labels for the convenience of the user. The Address, Data, and Status labels are used by the inverse assembler to generate assembly language mnemonics for display of the trace list. Pertinent control and clock threshold levels are also part of the format specification.

The logical NAND of CPU signals INTA, WR, and RD is used as the master clock signal to the logic analyzer.

ALE is used as the slave clock signal to the logic analyzer.

USER BASE

The User Base menu of the format specification is set up with names to identify values found on the status label. See figure 5.

State Format Specification		
[User Base]		
State Labels		
Value	STAT	
[BIN]		
0000		
0001	memwr	(memory_write)
0010	memrd	(memory_read)
0011	opfch	(opcode_fetch)
0100		
0101		
0110		
0111		
1000		
1001	io wr	(I/O_write)
1010	io rd	(I/O_read)
1011	intak	(interrupt acknowledge)
1100		
1101		
1110		
1111		

Figure 4. 8085 Status Map

8085 Inverse Assembler

The 8085 Inverse Assembler has been constructed so mnemonic output will resemble actual assembly source code. The few exceptions to this rule are detailed in the paragraphs below.

A pair of asterisks (**) displayed in the operand field of an instruction indicates that one byte of an expected (single or double byte) operand was not stored in the logic analyzer memory. Two pairs of asterisks (****) indicate that both bytes of a double byte operand were not stored.

If the standard 8085 trace and format specifications (from the 8085 configuration file) are used for making measurements, asterisks will be displayed when a conditional jump or conditional call instruction is evaluated to be false. The number of operand fetches (memory reads) performed is dependent upon the evaluation result.

If the evaluation is true, two operand fetches will produce the address to which program control will be passed. No asterisks will be displayed since both bytes of the operand will be present. If the evaluation is false, only one operand is fetched before control is passed to the next address in sequence. Since one of the two operands is missing, a pair of asterisks will be displayed instead of the (missing) high order byte.

Examples:

JNZ	0357	indicates that since the non-zero (NZ) condition was true, the jump to 0357H will occur.
JNZ	**57	indicates that since the non-zero (NZ) condition was false, the jump will not occur.

In the case that the conditional call or jump occurs at the end of logic analyzer memory, asterisks will be displayed for each byte of the operand not found in logic analyzer memory.

If the standard 8085 trace and format specification is used for a measurement these asterisks provide a convenient method to determine whether or not a conditional call or jump was executed.

In general, asterisks indicate that expected operand fetches are not stored in logic analyzer memory. If the standard 8085 trace and format specifications are not utilized, missing operand fetches can be due to the use of storage qualification.

Error Messages

The following list of messages will aid the user in identifying operation errors.

- Data Error - trace data collected by the logic analyzer cannot be retrieved from memory. Indicates hardware error or inverse assembler software error.
- Illegal Opcode - undefined opcode encountered. Result is indeterminate.

Note

Make no modifications to the ADDRESS, DATA, or STATUS labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Note also that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

8085 Inverse Assembler with General Purpose Probes

In order to use the inverse assembler for probes the general purpose probes must be connected to the 8085 microprocessor as shown in Table 3. After the specified hookups have been completed, data sampling may begin. Be sure to load the file "I8085IP". Once the inverse assembler has been loaded, the user must make the clock selection for general purpose probes. When the disc is read, the format specification for the 8085 is automatically set up. This format specification corresponds with the above hookup specification.

To obtain all three inputs required for the J clock (Master Clock) supply an external NAND gate, and wire it as follows: connect pins 11, 31, and 32 of the 8085 to inputs of NAND gate. Then supply the output of the NAND gate to the J clock on POD 4. Select L down (↓) for the slave clock.

If you do not need to include interrupt-acknowledge cycles in your analysis, you can obtain the Master Clock without using external circuitry. Connect 8085 pin 31 to the K clock of POD 3, and 8085 pin 32 to the J clock of POD 4. Then select positive-going transitions on the J and K clocks in the CLOCK field below the Master Clock in the Format Specification. Select L down (↓) for the slave clock.

Table 3. 8085 Signal List for General Purpose Probe Connections.

1630A/D & 1631A/D		1630G		8085 pin	pin mnemonic
POD	PROBE	POD	PROBE		
1	0	5	0	12	AD0
1	1	5	1	13	AD1
1	2	5	2	14	AD2
1	3	5	3	15	AD3
1	4	5	4	16	AD4
1	5	5	5	17	AD5
1	6	5	6	18	AD6
1	7	5	7	19	AD7
2	0	2	0	12	AD0
2	1	2	1	13	AD1
2	2	2	2	14	AD2
2	3	2	3	15	AD3
2	4	2	4	16	AD4
2	5	2	5	17	AD5
2	6	2	6	18	AD6
2	7	2	7	19	AD7
2	8	2	8	21	A8
3	0	3	0	22	A9
3	1	3	1	23	A10
3	2	3	2	24	A11
3	3	3	3	25	A12
3	4	3	4	26	A13
3	5	3	5	27	A14
3	6	3	6	28	A15
3	7	3	7	not used	-----
3	8	3	8	not used	-----
4	0	4	0	29	S0
4	1	4	1	33	S1
4	2	4	2	38	HLDA
4	3	4	3	34	IO/LM
1	GND	5	GND	20	GND
2	GND	2	GND	20	GND
3	GND	3	GND	20	GND
4	GND	4	GND	20	GND
2	L CLK	2	L CLK	30	ALE
4	J CLK	4	J CLK	11,31,32	INTA, WR, RD

Appendix A

Copyfile Utility Program

In addition to the inverse assemblers, the flexible disc contains a utility program COPYFILE which provides the 1630 or 1631 user a method of copying 1630 or 1631 executable programs and inverse assemblers from one disc to another.

Copyfile is an extension of the Storage Operation capabilities of the 1630 and 1631 which are limited to copying only non executable programs. An example of a non executable program would be a timing file.

To use the Copyfile, load it using the same loading procedure described in the "Operation" section of this Operating Note or the procedures in the 1630 or 1631 Operating and Programming manual. Once loaded, the program is initiated by pressing the INSERT key.

Once the program starts, the 1630 or 1631 display will ask for: copy FROM file name, file TYPE, bus address and unit number. When these have been specified, press INSERT again to load the file to be copied. When the copy FROM file has been loaded, the 1630 or 1631 will display all the same information in the copy TO fields as a default. The file name, bus address, and unit number can be re-specified if desired, however, the file type must remain the same as the file being copied.

To exit the Copyfile program, move the cursor to the EXIT field and press either the NEXT ☐ or PREV ☐ key.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of 1 year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. However, warranty service for products installed by HP and certain other products designated by HP will be performed at Buyer's facility at no charge within the HP service travel area. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and buyer shall pay HP's round trip travel expenses.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED, HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For assistance, contact your nearest Hewlett-Packard Sales and Service Office.

COPYRIGHT HEWLETT-PACKARD COMPANY 1984
COLORADO SPRINGS DIVISION
COLORADO SPRINGS, COLORADO, U.S.A.

ALL RIGHTS RESERVED

